EFFECT OF CLOCK NOISE ON THE SYNCHRONIZATION PERFORMANCE OF CONSTANT BIT RATE (CBR) TRAFFIC IN AN ATM NETWORK

T. Jayawardena and C. Olszewski
AT&T Labs
101 Crawford Corner Rd.
Holmdel, NJ 07733

Abstract

When Constant Bit Rate (CBR) traffic with an associated frequency is carried over an ATM network, the frequency needs to be reconstructed at the exit node of the ATM network. One method for reconstructing this frequency is the Synchronous Residual Time Stamp (SRTS) method. This method relies on two synchronized clocks, one at the entrance and the other at the exit of the ATM network.

This paper quantifies the synchronization performance of the signal leaving the ATM network when different levels of noise are present in the signal source clock, the clock at the entrance to the ATM network, or the clock at the exit of the ATM network. Simulations were performed to study the effects of these noise sources separately and in combination. The SRTS scheme itself generates noise with a characteristic time deviation (TDEV) signature. The noise on the signal leaving the ATM network is determined by both the SRTS signature noise and the noise of clocks in the entrance and exit nodes of the ATM network. As the noise of the clocks rise above certain levels, the noise on the signal tends to be determined more by the clock noise than the inherent noise from the SRTS scheme.

INTRODUCTION

A key advantage of Asynchronous Transfer Mode (ATM) networks from a telecommunications carrier's perspective is the ability to carry voice, video, and data traffic on a single network. This is achieved by segmenting the voice, video, or data traffic stream into small units and sending them across the ATM network in 53-byte ATM cells. User information, i.e. voice, video, or data, is converted into ATM cells at the entrance to the ATM network and reconverted to the original format at the exit of the ATM network.

The small constant size of ATM cells makes it possible to achieve the desired Quality of Service (QoS) for different types of traffic carried over an ATM network. QoS is a term used to characterize the transmission characteristic requirements of different types of ATM traffic. The most stringent QoS is needed to carry Constant Bit Rate (CBR) user information. CBR traffic has a frequency associated with the bit rate of the signal which needs to be reconstructed at the exit node of the ATM network. There are two popular

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methods for achieving this: The adaptive method and the Synchronous Residual Time Stamp (SRTS) method.

In the adaptive method, the cell inter-arrival times are averaged at the exit node of the network to reconstruct the original bit rate. Although at the entrance of the ATM network cells carrying the CBR traffic are generated periodically, their transit times through the network are not constant due to Cell Delay Variation (CDV) encountered within the network. When the adaptive method is used, low frequency CDV, which cannot be removed by averaging, will degrade the synchronization performance of the exiting signal.

The SRTS method relies on two synchronized clocks, that is, two clocks having the same average frequency, one at the entrance and the other at the exit of the ATM network. (Strictly speaking, the clocks are only "syntonized," i.e. have the same frequency. Keeping with telecommunications' parlance we shall use "synchronization" to mean "syntonization,") Bits of the incoming CBR traffic are periodically assigned a time stamp upon entrance to the ATM network. This time stamp is sent along with the information bits to the exit node of the ATM network. There, the time stamp and exit clock are used to recreate the frequency of the signal leaving the ATM network. This scheme is illustrated in Figure 1. An important advantage of the SRTS scheme is that the synchronization performance of the signal exiting the ATM network is largely insensitive to CDV. However, the synchronization performance of the signal is affected by the behavior of the clocks at the entrance and exit nodes of the ATM network. The objective of this study is to understand the effect of different levels of clock noise on the synchronization performance of the signal exiting the ATM network when SRTS method is used to reconstruct the signal frequency. See [1] for details of the SRTS method.

THE SIMULATION MODEL

We consider two architectures for synchronizing the clocks at the entrance and exit of the ATM network. These synchronization architectures will induce different levels of noise on the clocks used in the SRTS method. The two synchronization architectures are the following:

1. Each node is synchronized by a stratum 2 or stratum 3 Building Integrated Timing Supply (BITS) clock, which is directly synchronized by a collocated Primary Reference Source (PRS)
2. Each node is synchronized by a reference signal from a remote PRS.

The BITS clock is the most accurate and stable clock at a given location. It is used as the reference to which all other collocated clocks are synchronized. A PRS is a clock which has a long-term accuracy of one part in 1011 with verification to UTC ([2]). The two synchronization architectures are shown in Figure 2.

We use TDEV masks to specify different levels of clock noise. TDEV is the square root of TVAR. (See [7] for details of TVAR and its relation to other variances). The ANSI T1.101 TDEV mask for wander generation of a stratum 2 or 3 clock (see [2]) is used as the maximum level of noise in clocks at the entrance and exit nodes of the network when a collocated PRS is used to synchronize the BITS clocks at these nodes (case 1). When the nodes are synchronized by a remote PRS (case 2), we use two TDEV masks to simulate two levels of maximum noise in the node clocks. The higher level of noise is taken from the TDEV interface mask of T1.101 [2] and the lower level of noise is from the TDEV mask of T1.105.09 [3]. These three TDEV masks are shown in Figure 3.

We used two methods of generating clock noise from the TDEV masks: The fractional Brownian motion method in [4] and the successive random additions method in [5]. The method in [4] is memory-intensive and is better suited for simulations of short time periods. The method in [5] was used for longer simulation periods (integration times of thousands of seconds).

We used the DS1 (Digital Signal level 1 in the North American Digital Hierarchy) with an associated nominal bit rate of 1.544 Mbps as the CBR signal entering the ATM network.

SIMULATION RESULTS

The SRTS method itself induces noise on the signal exiting the ATM network even when there is no noise present in the clocks of the entrance and exit nodes. The attributes of this induced noise depend on the frequency of the signal entering the ATM network, as well as the frequency of the network clock used to construct the time stamps. However, most of the power of this SRTS "signature" noise is in the high frequency region and most of it will be attenuated by a low-pass filter in actual SRTS implementations. The TDEV signatures are shown in Figure 4 for two cases: (a) The DS1 entering the ATM network has a nominal frequency (1.544 MHz) (b) the DS1 entering the ATM network has a +30Hz offset from the nominal frequency. A network clock frequency of 2.43MHz was used in all simulations.

To see how clock noise affects the DS1 phase in the SRTS method, we used the TDEV curves given in Figure 5 to simulate clocks with high, intermediate, and low levels of noise relative to the SRTS signature noise.

The TDEV of the DS1 exiting the ATM network follows the SRTS signature TDEV up to some integration time (in the higher frequency region) and then follows the clock noise TDEV for larger values of integration time (in the lower frequency region). The higher the noise level, the sooner the DS1 phase TDEV begins to follow the noise TDEV. Figure 6(a) (for a DS1 with the nominal frequency) and Figure 6(b) (for a DS1 with a +30 Hz offset) show these trends.

Next, we simulated the synchronization performance of the DS1 exiting the ATM network when the clock noise is generated according to various ANSI T1 TDEV masks ([2], [3]). Figure 7 shows the TDEV of a simulated clock and the TDEV mask used to generate the clock noise. The high degree of coincidence of the two TDEV curves show that the generated clock noise is consistent with the corresponding TDEV mask. Simulated noise from the other two TDEV masks showed a similar consistency.

Figure 8(a) and Figure 8(b) show the TDEV of the simulated DS1 phase resulting from clock noise generated from different TDEV masks. The TDEV of the DS1 phase approximately follows the TDEV of the clocks.

Finally, we also investigated the effect of noise in the source input signal on the performance of the timing of the signal recreated at the exit node. The TDEVs of the source signals having low, intermediate, and high levels of noise for this part of the study are shown in Figure 9. Figure 10 shows the TDEVs of the simulated phase of the DS1 at the exit node, subject to the various levels of source noise. Figure 10 also includes the intrinsic SRTS noise signature.

The behavior of the TDEV curves for the phase of the DS1 is very similar to the behavior of the curves for the DS1 produced when there is noise on the network clocks (Figure 6). At small integration times (high frequencies), the curves more or less follow the characteristic curve of the SRTS method. As the integration time of the TDEV is increased further, signals with more noise depart from the characteristic SRTS curve sooner than signals with less noise. In all cases, once the TDEV curve of a DS1's phase departs from the SRTS curve, it remains at noise levels characteristic of the noise generated on the source.

At small integration times, there appears to be some filtering of the source noise on the DS1 at the exit node. This effect is explained by the operation of the SRTS method, in which a single time stamp represents the time at which 3,008 bits have been received at the entrance node. Low-to-moderate levels of noise at time scales less than that of the 3,008-bit frame are eclipsed by the signature of the SRTS method itself. High levels of noise at these time scales will be attenuated by this effect, but will produce more noise than the signature of the SRTS method. A low-pass filter in a realistic implementation of the SRTS method would reduce the high-frequency peak of the method, and would presumably attenuate this short-time-scale noise further.

CONCLUSIONS

The SRTS method introduces noise on to the DS1 phase leaving the ATM network even when there is no noise in the entrance and exit node clocks. The attributes of this noise depend on the frequency of the signal entering the ATM network and the frequency of the network clock used to construct the time stamps. Most of this SRTS "signature" noise power is in the high frequency and will be attenuated by a low-pass filter used in SRTS implementations.

When there is noise in the entrance and exit node clocks, the TDEV of the DS1 phase follows the SRTS TDEV "signature" only in the high frequency region and begins following the noise TDEV in the lower frequency region. The higher the level of clock noise, the higher the threshold frequency at which the TDEV of DS1 phase begins to follow the clock noise TDEV. This behavior is also evident when there is noise on the source signal itself.

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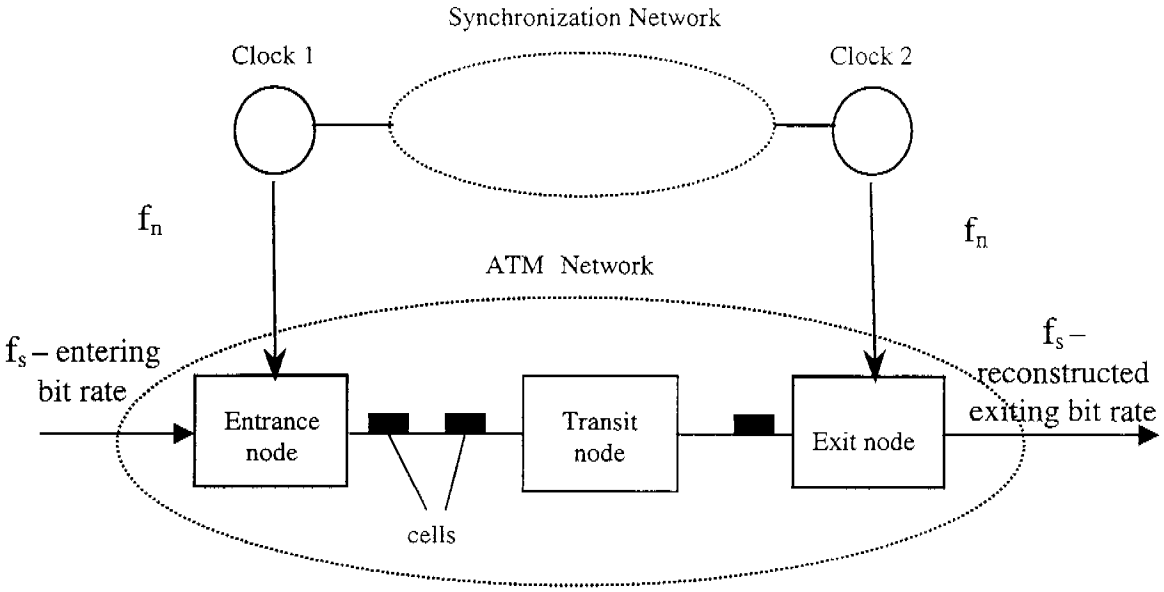


Figure 1. SRTS method for transporting CBR traffic over an ATM network.

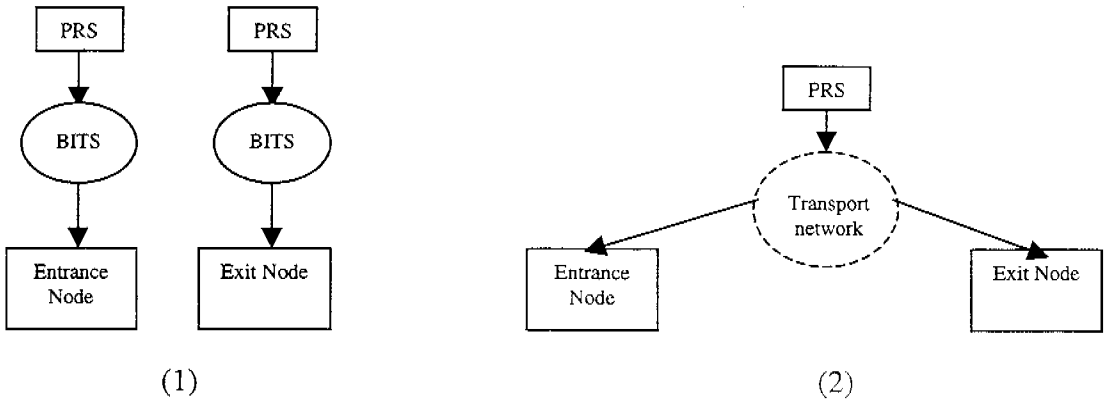


Figure 2. Two architectures for synchronizing the entrance and exit node clocks.

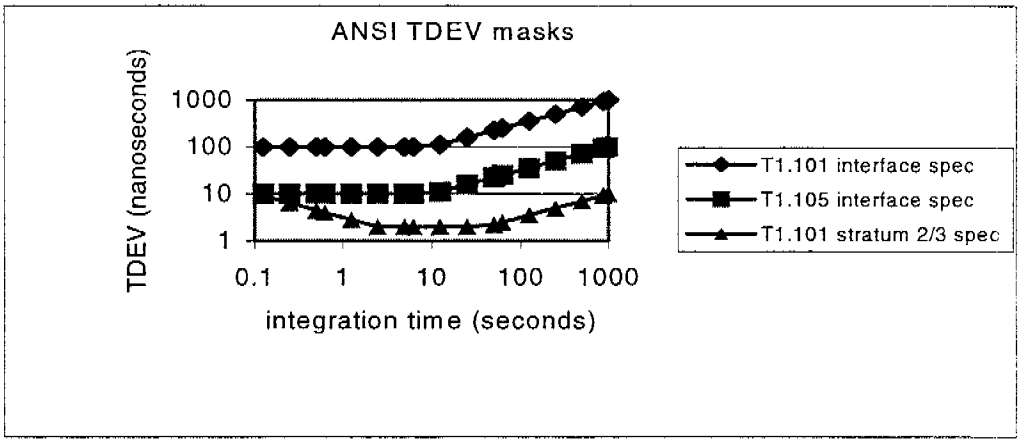


Figure 3. ANSI TDEV masks used to simulate clock noise.

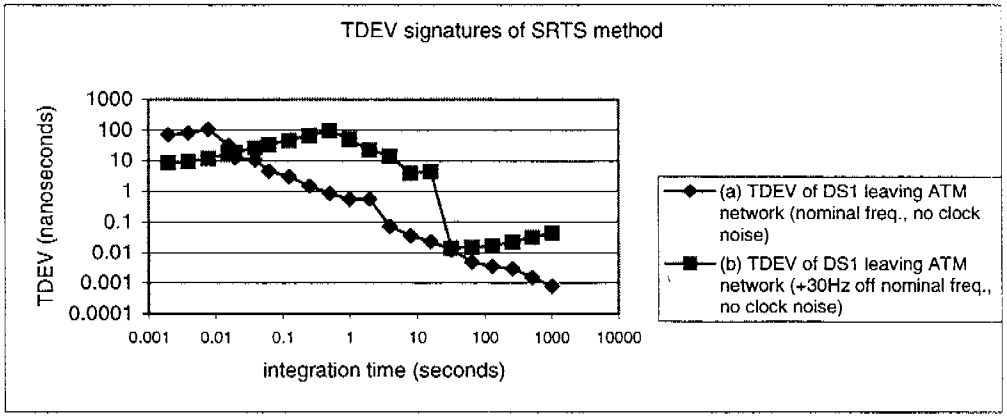


Figure 4. TDEV of DS1 leaving ATM network when there is no noise in any clock:
(a) entering DS1 has nominal frequency
(b) entering DS1 has +30Hz frequency offset from nominal.

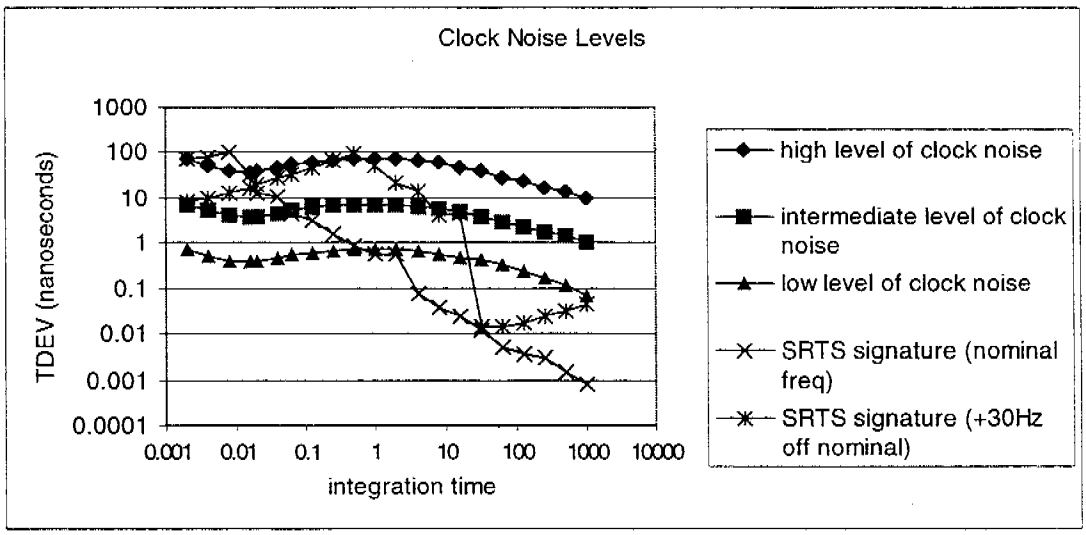
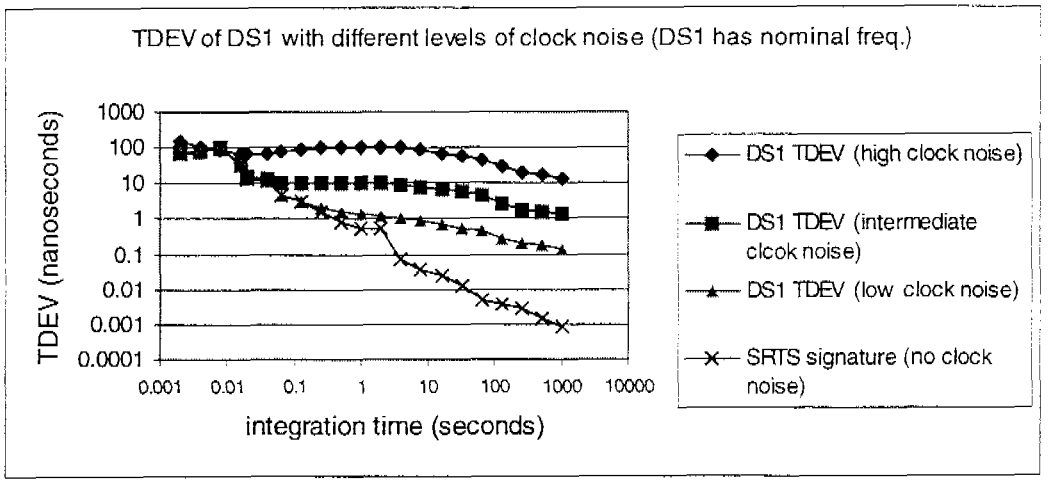


Figure 5. TDEV of different levels of clock noise and TDEV of the SRTS signatures.

(a)



(b)

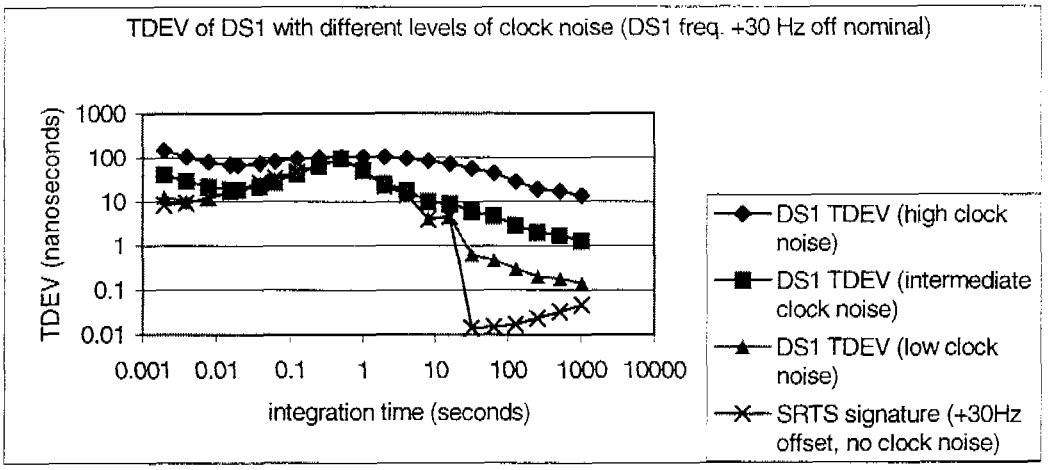


Figure 6. TDEV of DS1 phase resulting from different levels of clock noise
(a) Entering DS1 has nominal frequency
(b) Entering DS1 has +30 Hz offset from nominal frequency.

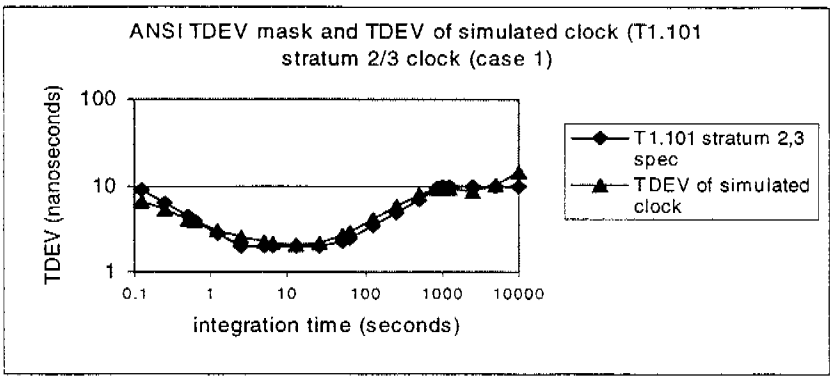
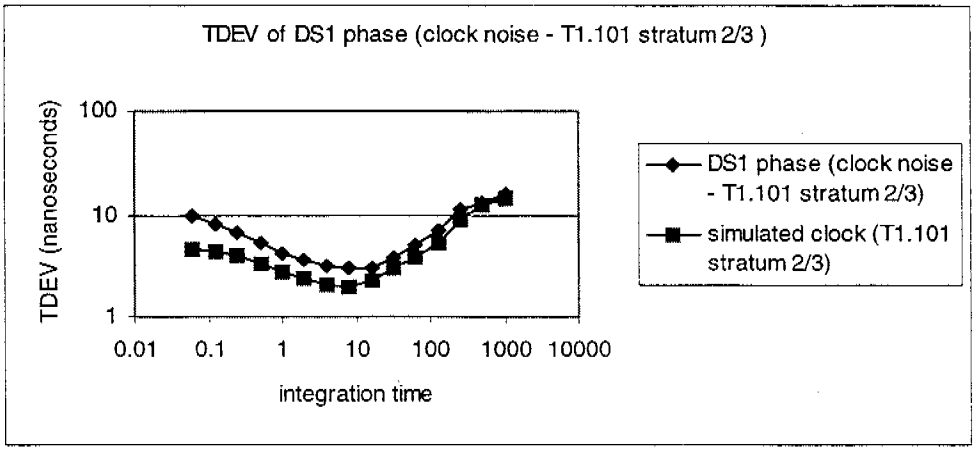


Figure 7. TDEV mask used to simulate the clock noise and TDEV of simulated clock (T1.101 stratum 2 or stratum 3 clock).

(a)



(b)

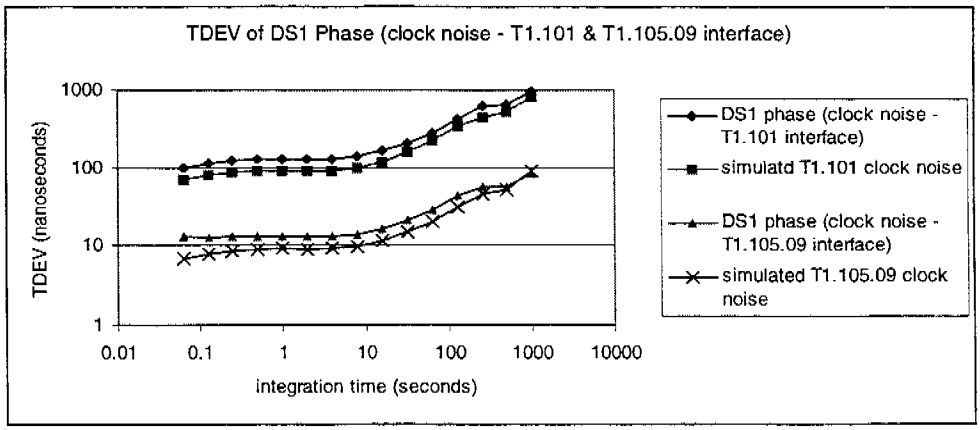


Figure 8. TDEV of simulated DS1 resulting from clock noise
(a) Generated from T1.101 stratum 2/3 TDEV mask
(b) Generaged from T1.101 and T1.105.09 interface TDEV masks.

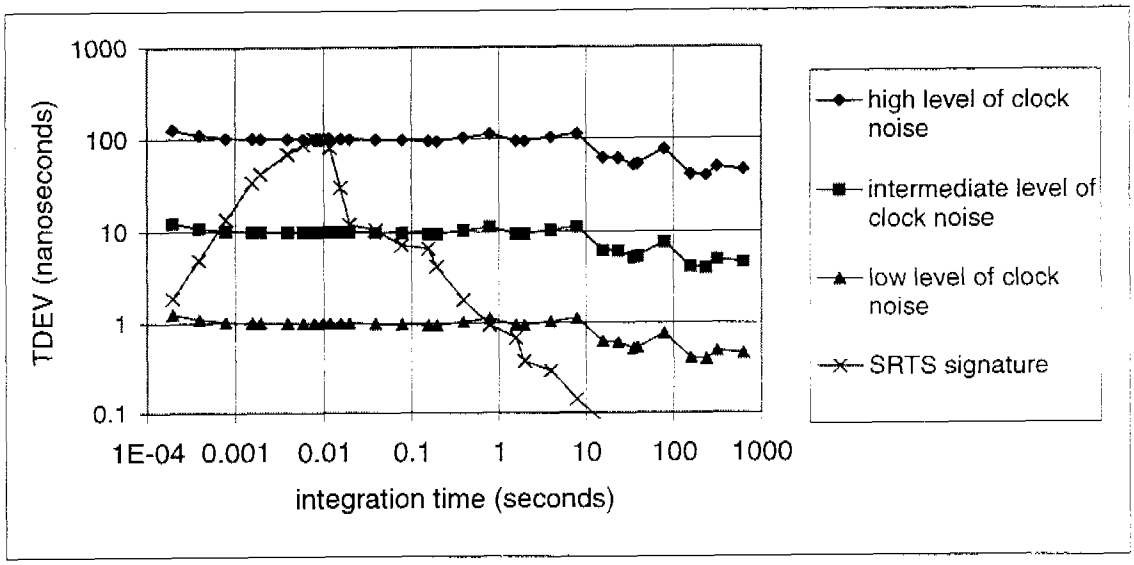


Figure 9. TDEV of various levels of source noise.

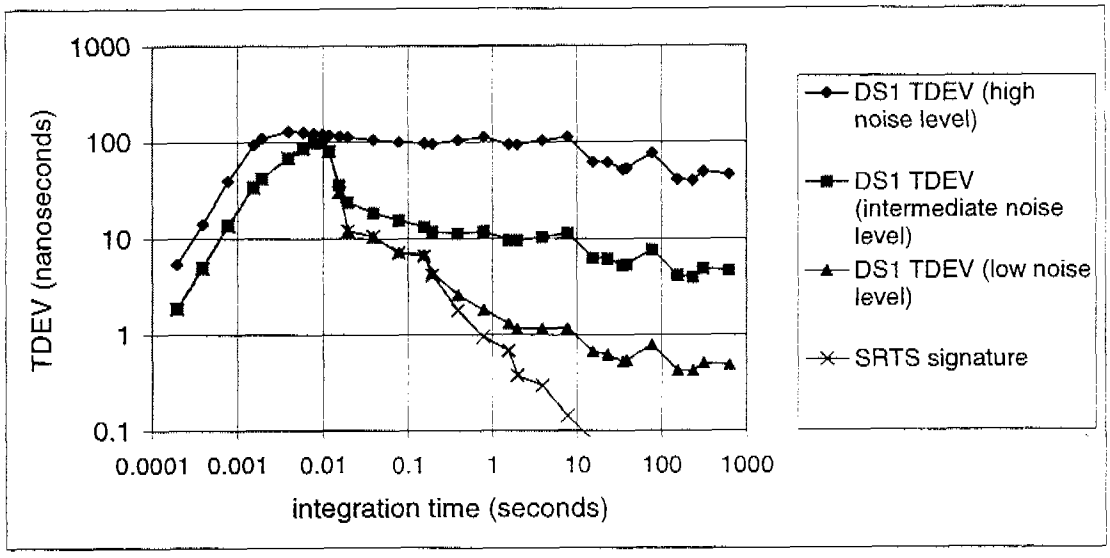


Figure 10. TDEV of DS1 phase resulting from various levels of noise on source.